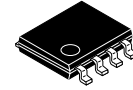


Half-Bridge Gate Driver

FAN7380


SOIC8
(8-SOP)
CASE 751EG

Description

The FAN7380 is a monolithic half-bridge gate-drive IC for MOSFETs and IGBTs that operate up to +600 V. onsemi's high-voltage process and common-mode noise cancelling technique provide stable operation of high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V. The input logic level is compatible with standard TTL-series logic gates. The internal shoot-through protection circuit provides 100 ns dead-time to prevent output switching devices from both conducting during transition periods. UVLO circuits for both channels prevent malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. Output drivers typically source / sink at 90 mA / 180 mA, respectively, which is suitable for fluorescent / compact fluorescent lamp ballast applications and systems requiring low di/dt noise.

Features

- Floating Channel Designed for Bootstrapping Operation to +600 V
- Typically 90 mA / 180 mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Cancelling Circuit
- Extended Allowable Negative V_S Swing to -9.8 V for Signal Propagation at $V_{CC} = V_{BS} = 15$ V
- V_{CC} & V_{BS} Supply Range from 10 V to 20 V
- UVLO Functions for Both Channels
- TTL-Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50 ns
- Built-in 100 ns Dead-Time Control Function
- Output In-Phase with Input Signal
- This is a Pb-Free Device

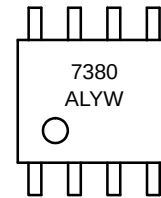
Typical Applications

- Fluorescent Lamp Ballast
- Compact Fluorescent Lamp Ballast

Related Resources

- <https://www.onsemi.com/pub/collateral/an-6076.pdf>
- <https://www.onsemi.com/pub/collateral/an-9052.pdf>
- <https://www.onsemi.com/pub/collateral/an-8102.pdf>

MARKING DIAGRAM



7380	= Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

FAN7380

TYPICAL APPLICATION CIRCUIT

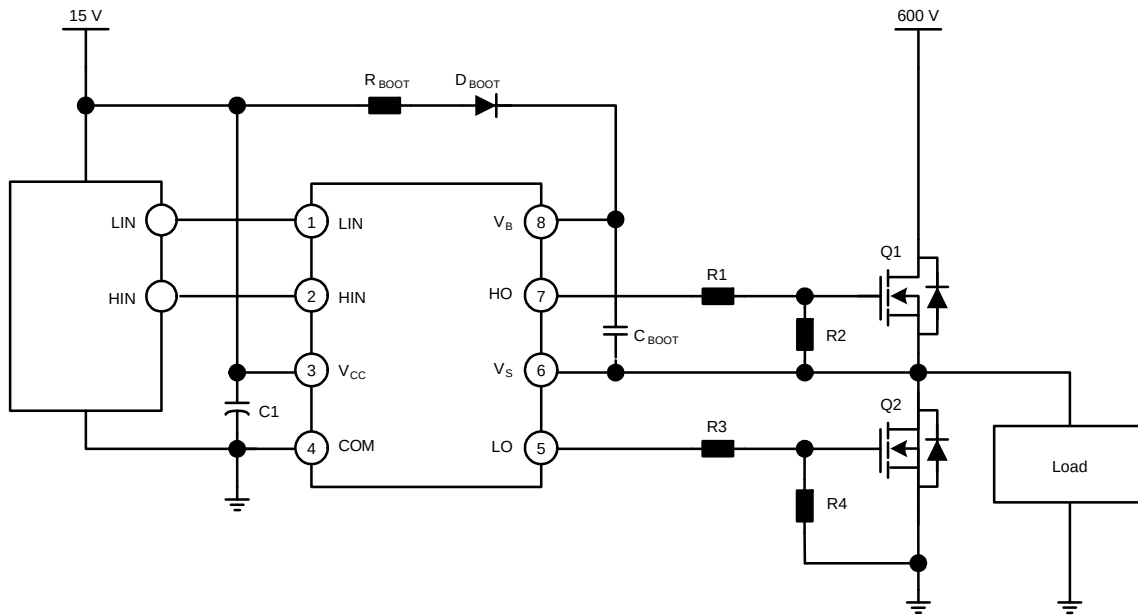


Figure 1. Application Circuit for Fluorescent Lamp Ballast

INTERNAL BLOCK DIAGRAM

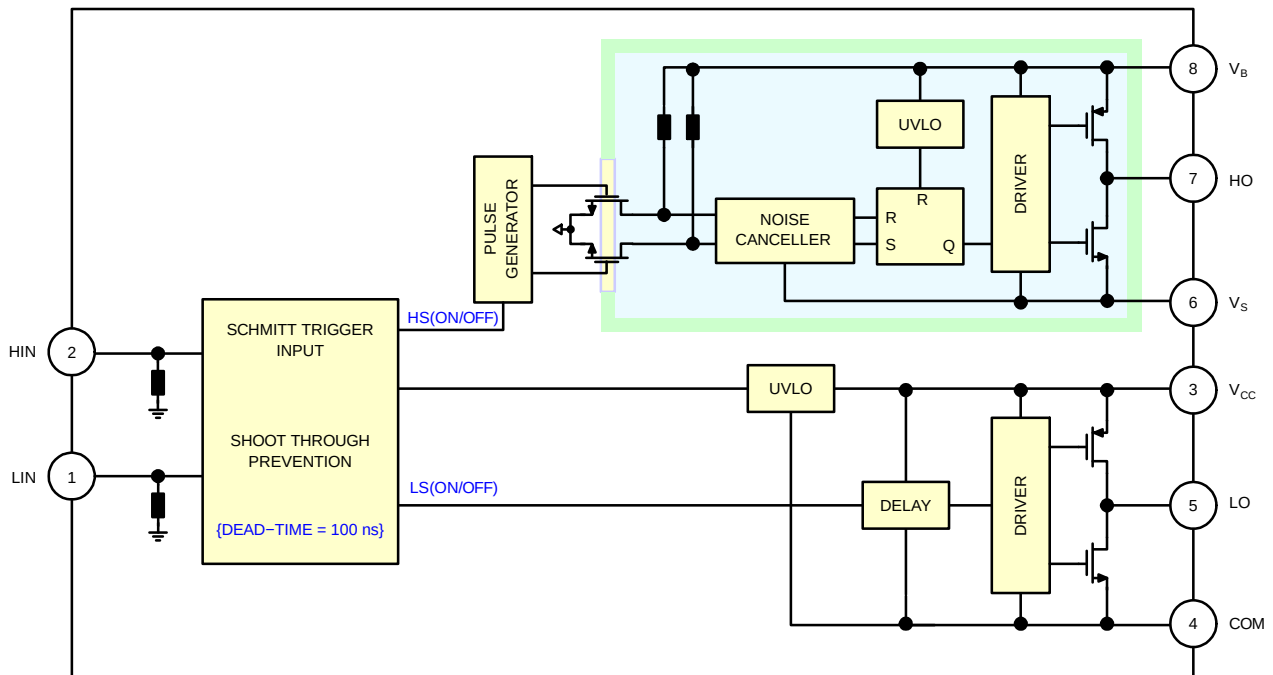


Figure 2. Functional Block Diagram

FAN7380

PIN CONFIGURATION

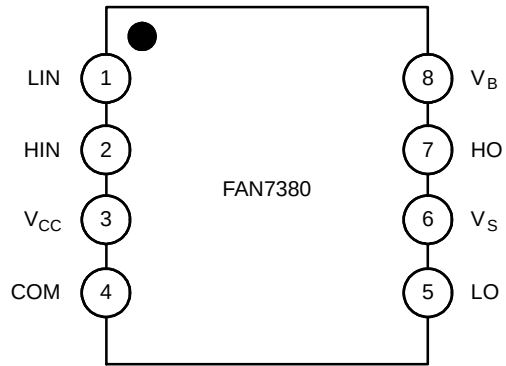


Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

Pin No.	Name	I/O	Description
1	LIN	I	Logic Input for Low-Side Gate Driver Output
2	HIN	I	Logic Input for High-Side Gate Driver Output
3	V _{CC}	I	Low-Side Supply Voltage
4	COM		Logic Ground and Low-Side Driver Return
5	LO	O	Low-Side Driver Output
6	V _S	I	High-Voltage Floating Supply Return
7	HO	O	High-Side Driver Output
8	V _B	I	High-Side Floating Supply

FAN7380

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V _S	High-side Offset Voltage	V _B – 25	V _B + 0.3	V
V _B	High-side Floating Supply Voltage	–0.3	625.0	
V _{HO}	High-side Floating Output Voltage HO	V _S – 0.3	V _B + 0.3	
V _{CC}	Low-side and Logic-fixed Supply Voltage	–0.3	25.0	
V _{LO}	Low-side Output Voltage LO	–0.3	V _{CC} + 0.3	
V _{IN}	Logic Input Voltage (HIN, LIN)	–0.3	V _{CC} + 0.3	
COM	Logic Ground	V _{CC} – 25	V _{CC} + 0.3	
dV _S /dt	Allowable Offset Voltage Slew Rate	–	50	V/ns
P _D (Note 1, 2, 3)	Power Dissipation	–	0.625	W
θ _{JA}	Thermal Resistance, Junction-to-ambient	–	200	°C/W
T _J	Junction Temperature	–	150	°C
T _S	Storage Temperature	–50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
JESD51-2: Integral circuits thermal test method environmental conditions – natural convection
JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

RECOMMENDED OPERATING RATINGS

Symbol	Parameter	Min	Max	Unit
V _B	High-side Floating Supply Voltage	V _S + 10	V _S + 20	V
V _S	High-side Floating Supply Offset Voltage	6 – V _{CC}	600	
V _{HO}	High-side (HO) Output Voltage	V _S	V _B	
V _{LO}	Low-side (LO) Output Voltage	COM	V _{CC}	
V _{IN}	Logic Input Voltage (HIN, LIN)	COM	V _{CC}	
V _{CC}	Low-side Supply Voltage	10	20	
T _A	Ambient Temperature	–40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

FAN7380

STATIC ELECTRICAL CHARACTERISTICS ($V_{BIAS} (V_{CC}, V_{BS}) = 15.0 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CCUV+} V_{BSUV+}	V_{CC} & V_{BS} Supply Under-voltage Positive Going Threshold		8.2	9.2	10.0	V
V_{CCUV-} V_{BSUV-}	V_{CC} & V_{BS} Supply Under-voltage Negative Going Threshold		7.6	8.7	9.6	
V_{CCUVH} V_{BSUVH}	V_{CC} Supply Under-voltage Lockout Hysteresis		–	0.5	–	
I_{LK}	Offset Supply Leakage Current	$V_B = V_S = 600 \text{ V}$	–	–	50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{IN} = 0 \text{ V}$ or 5 V	–	44	100	
I_{QCC}	Quiescent V_{CC} Supply Current	$V_{IN} = 0 \text{ V}$ or 5 V	–	70	180	
I_{PBS}	Operating V_{BS} Supply Current	$f_{IN} = 20 \text{ kHz}$, rms value	–	–	600	μA
I_{PCC}	Operating V_{CC} Supply Current	$f_{IN} = 20 \text{ kHz}$, rms value	–	–	610	
V_{IH}	Logic “1” Input Voltage		2.5	–	–	V
V_{IL}	Logic “0” Input Voltage		–	–	0.8	
V_{OH}	High-level Output Voltage, $V_{BIAS}-V_O$	$I_O = 20 \text{ mA}$	–	–	2.8	V
V_{OL}	Low-level Output Voltage, V_O		–	–	1.2	
I_{IN+}	Logic “1” Input Bias Current	$V_{IN} = 5 \text{ V}$	–	5	40	μA
I_{IN-}	Logic “0” Input Bias Current	$V_{IN} = 0 \text{ V}$	–	1.0	2.0	
I_{O+}	Output HIGH Short-circuit Pulse Current	$V_O = 0 \text{ V}$, $V_{IN} = 5 \text{ V}$ with $PW \leq 10 \mu\text{s}$	60	90	–	mA
I_{O-}	Output LOW Short-circuit Pulsed Current	$V_O = 15 \text{ V}$, $V_{IN} = 0 \text{ V}$ with $PW \leq 10 \mu\text{s}$	130	180	–	
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		–	–9.8	–7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC ELECTRICAL CHARACTERISTICS ($V_{BIAS} (V_{CC}, V_{BS}) = 15.0 \text{ V}$, $V_S = \text{COM}$, $C_L = 1000 \text{ pF}$ and $T_A = 25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t_{on}	Turn-on Propagation Delay	$V_S = 0 \text{ V}$	70	135	200	ns
t_{off}	Turn-off Propagation Delay	$V_S = 0 \text{ V}$ or 600 V (Note 4)	60	130	190	
t_r	Turn-on Rise Time		160	230	290	
t_f	Turn-off Fall Time		20	90	160	
DT	Dead Time		80	120	190	
MT	Delay Matching, HS & LS Turn-on/off		–	–	50	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. This parameter guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

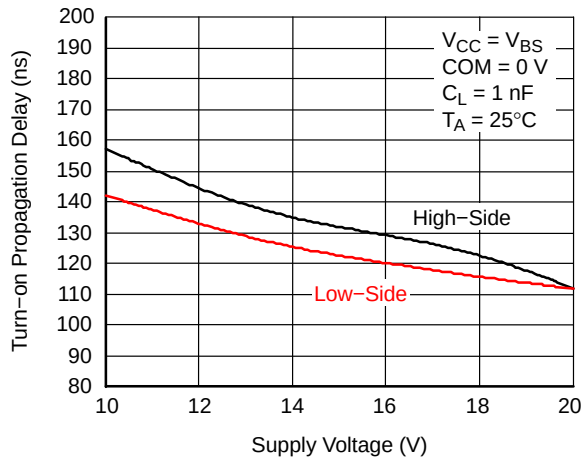


Figure 4. Turn-On Propagation Delay vs. Supply Voltage

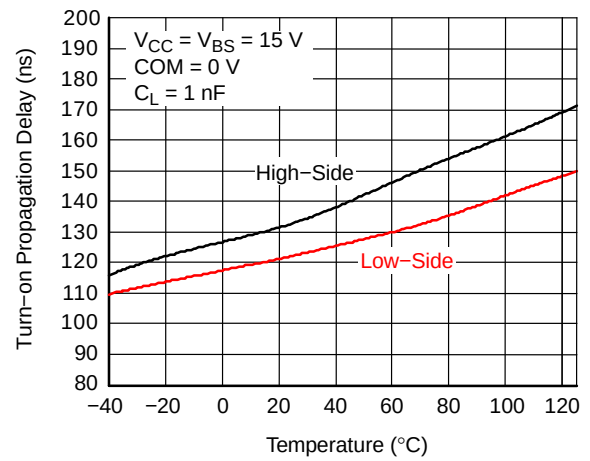


Figure 5. Turn-On Propagation Delay vs. Temperature

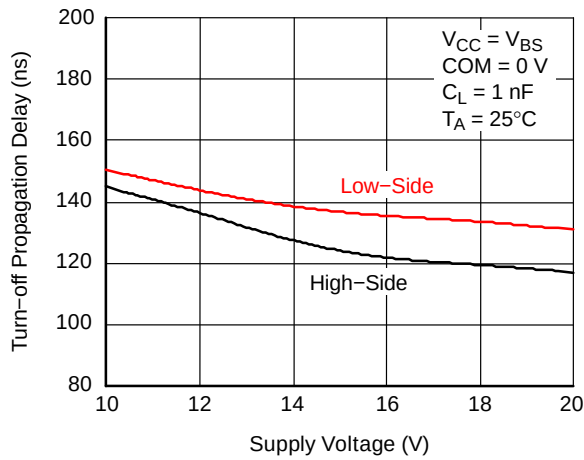


Figure 6. Turn-Off Propagation Delay vs. Supply Voltage

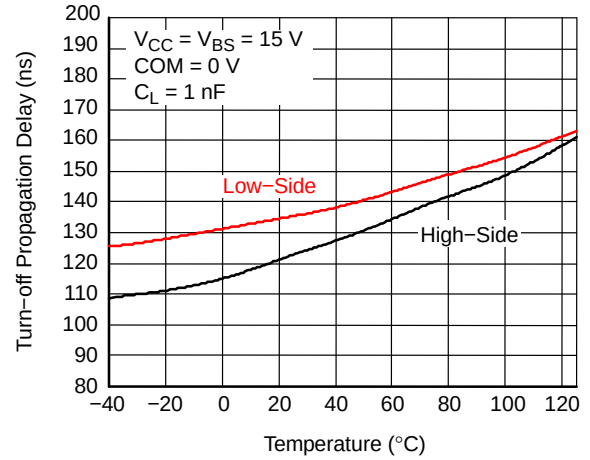


Figure 7. Turn-Off Propagation Delay vs. Temperature

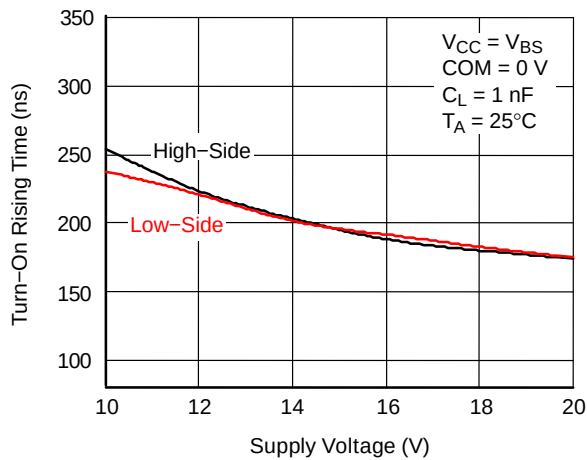


Figure 8. Turn-On Rising Time vs. Supply Voltage

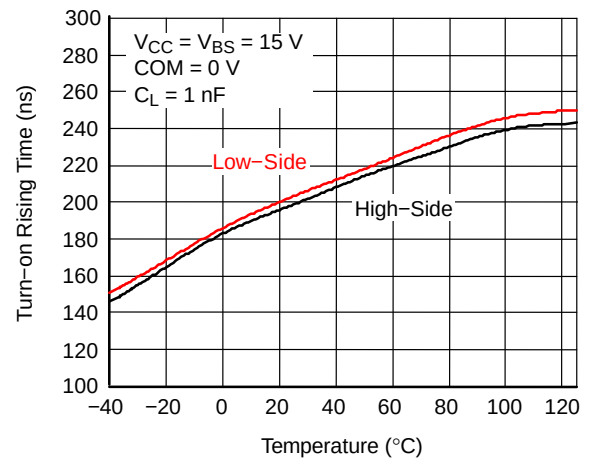


Figure 9. Turn-On Rising Time vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

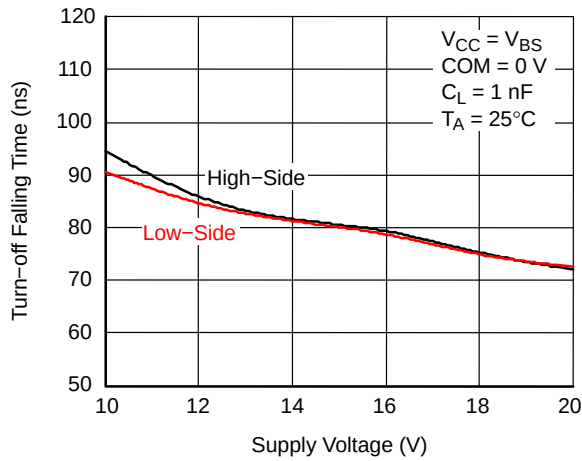


Figure 10. Turn-Off Falling Time vs. Supply Voltage

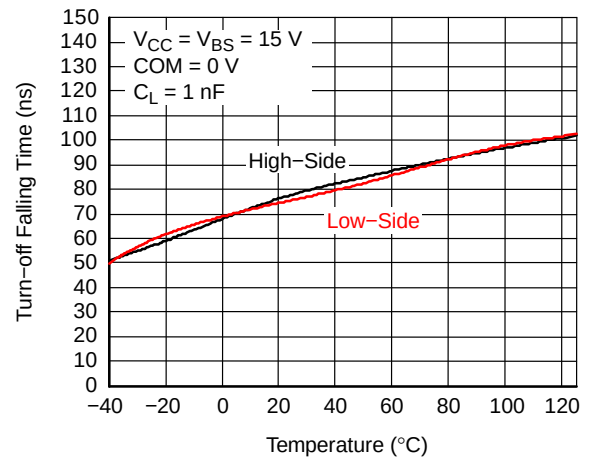


Figure 11. Turn-Off Falling Time vs. Temperature

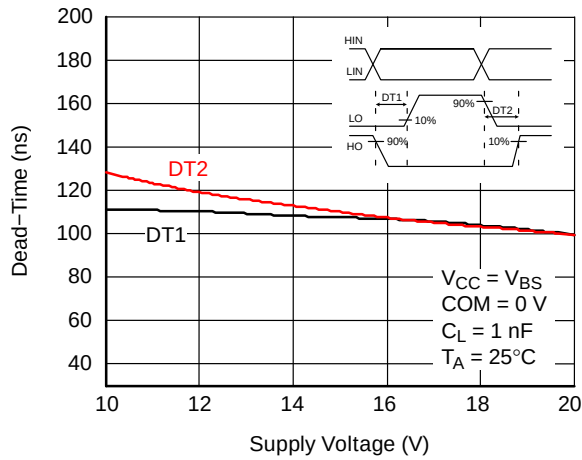


Figure 12. Dead-Time vs. Supply Voltage

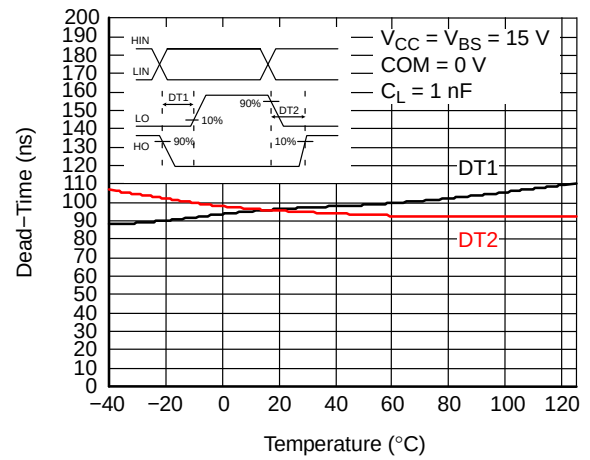


Figure 13. Dead-Time vs. Temperature

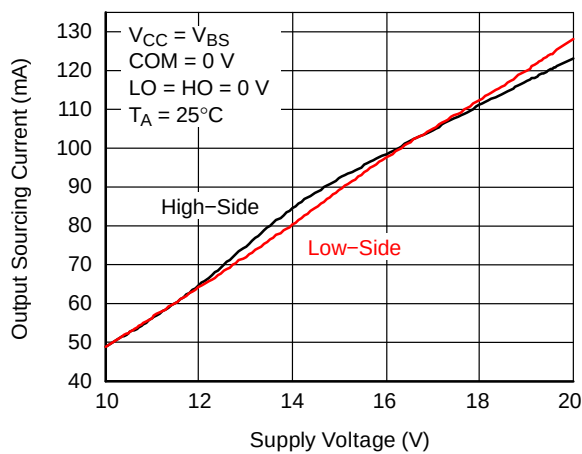


Figure 14. Output Sourcing Current vs. Supply Voltage

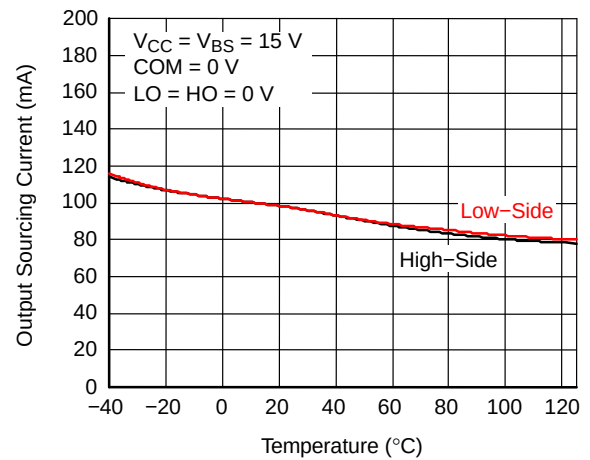


Figure 15. Output Sourcing Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

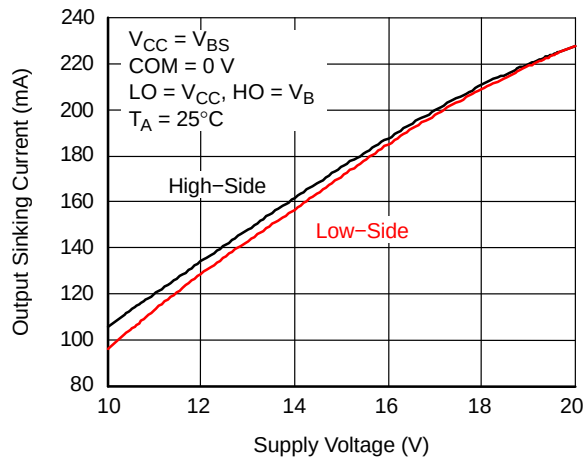


Figure 16. Output Sinking Current vs. Supply Voltage

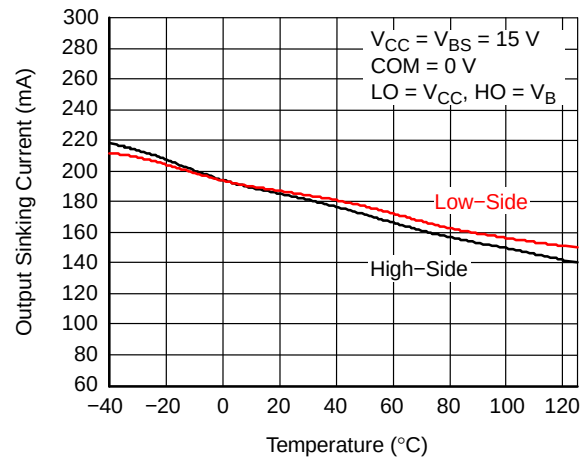


Figure 17. Output Sinking Current vs. Temperature

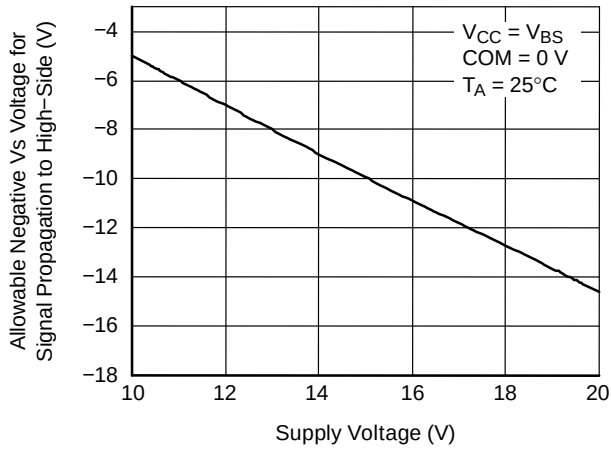


Figure 18. Allowable Negative Vs Voltage for Signal Propagation to High-Side vs. Supply Voltage

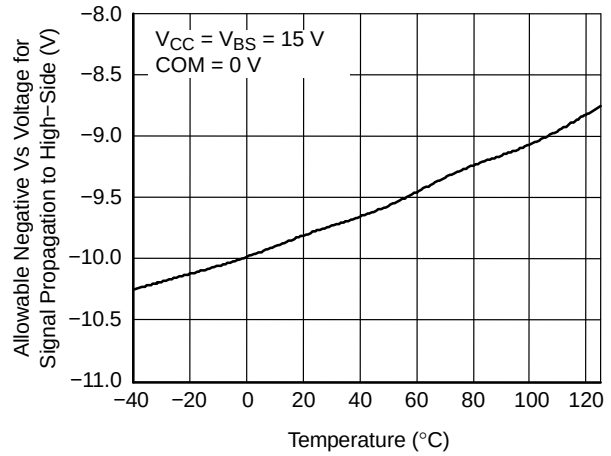
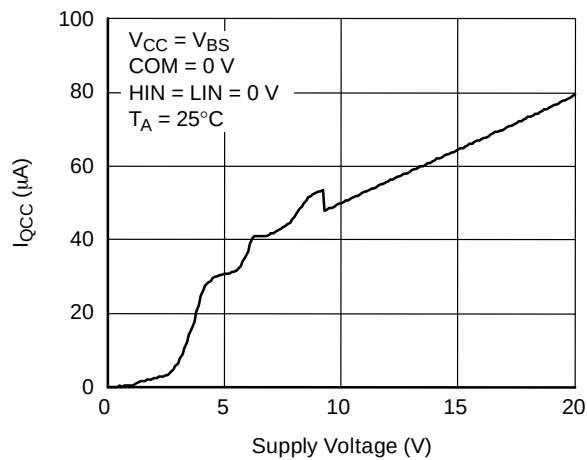
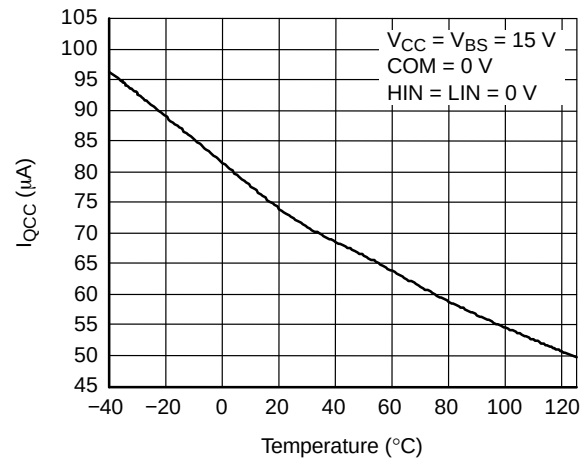


Figure 19. Allowable Negative Vs Voltage for Signal Propagation to High-Side vs. Temperature

Figure 20. I_{QCC} vs. Supply VoltageFigure 21. I_{QCC} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

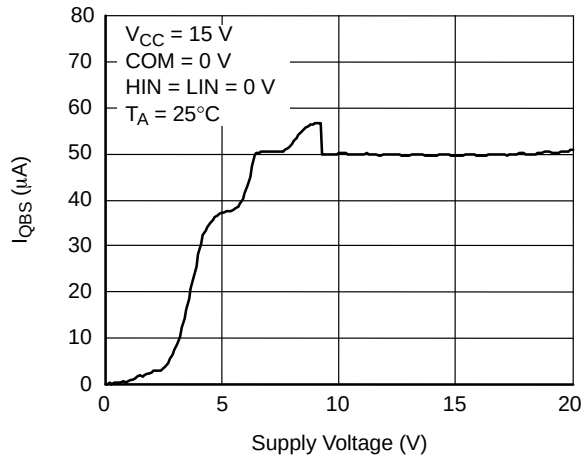
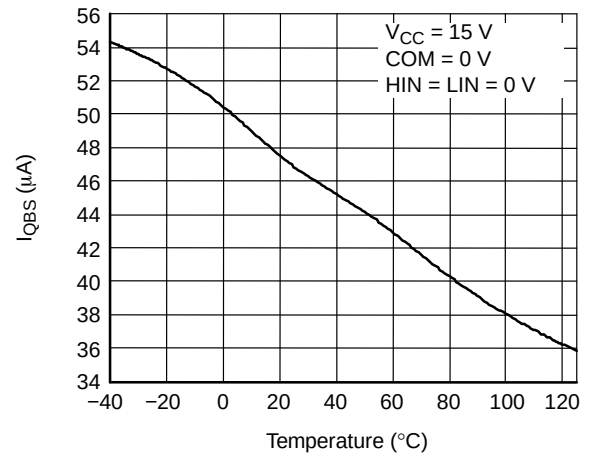
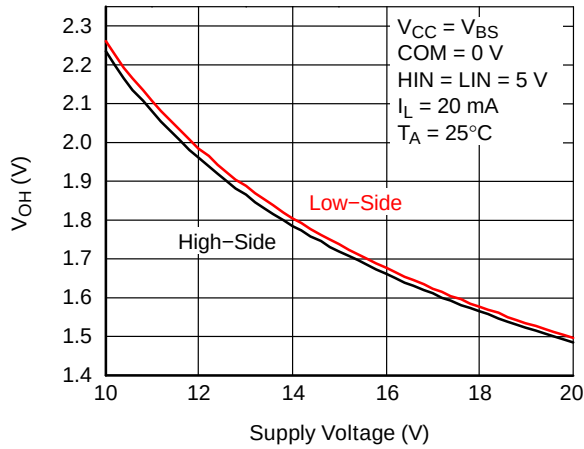
Figure 22. I_{QBS} vs. Supply VoltageFigure 23. I_{QBS} vs. Temperature

Figure 24. High-Level Output Voltage vs. Supply Voltage

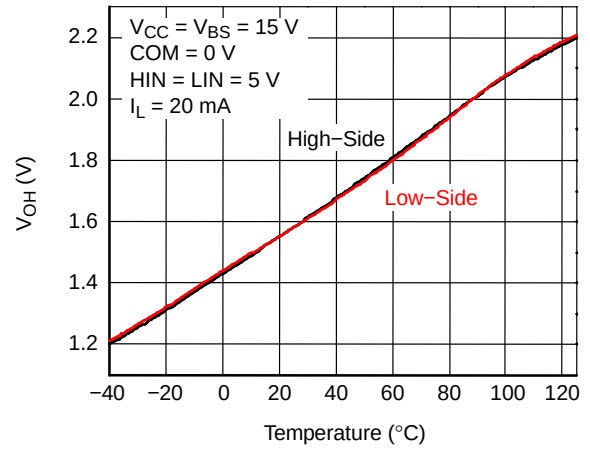


Figure 25. High-Level Output Voltage vs. Temperature

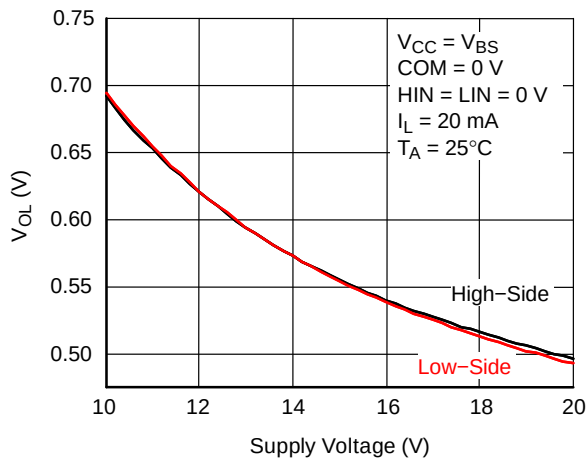


Figure 26. Low-Level Output Voltage vs. Supply Voltage

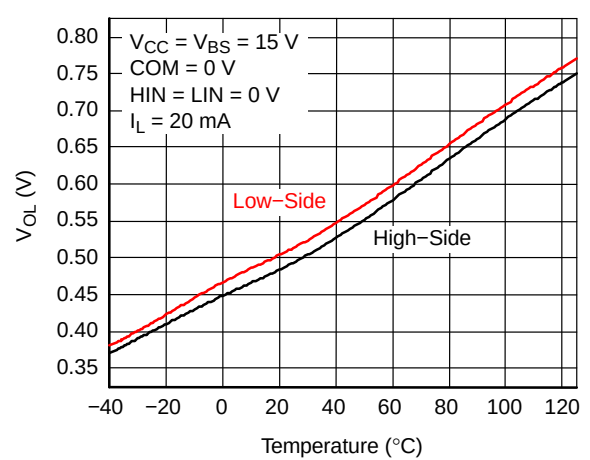


Figure 27. Low-Level Output Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

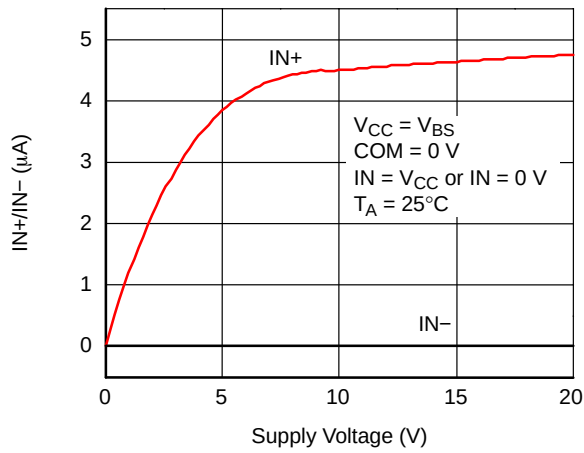


Figure 28. Input Bias Current vs. Supply Voltage

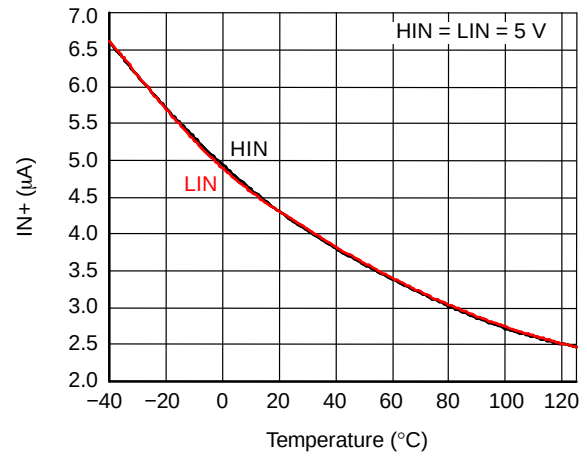


Figure 29. Input Bias Current vs. Temperature

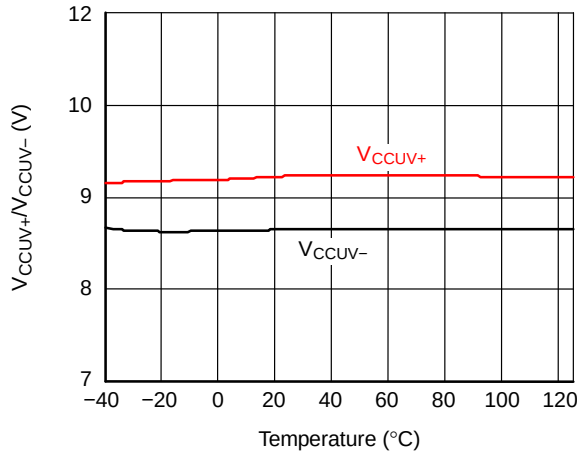
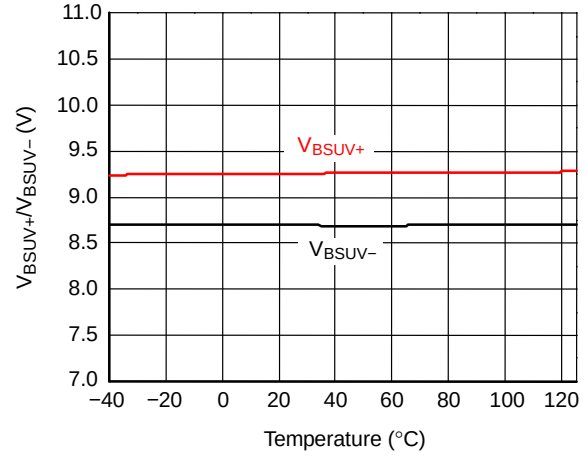
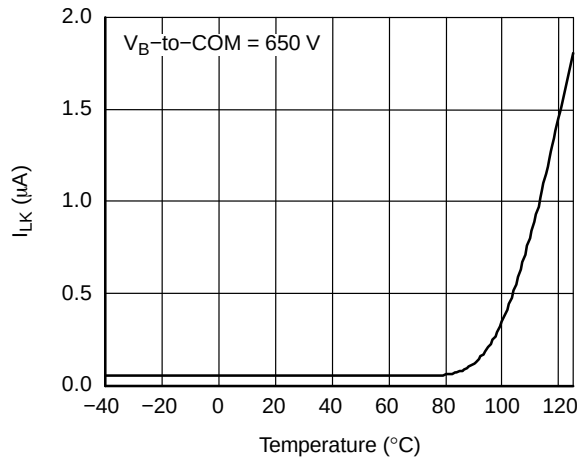
Figure 30. V_{CC} UVLO Threshold Voltage vs. TemperatureFigure 31. V_{BS} UVLO Threshold Voltage vs. Temperature

Figure 32. VB to COM Leakage Current vs. Temperature

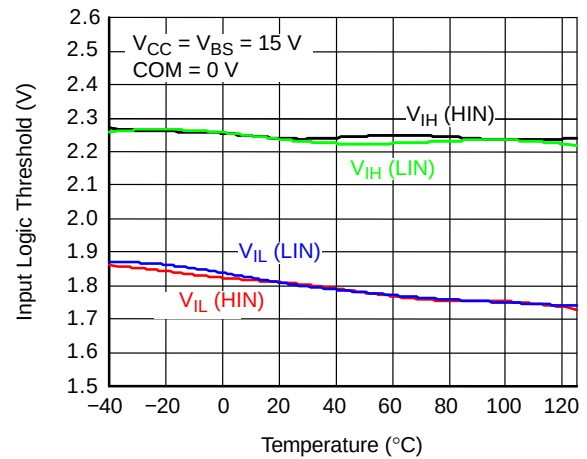


Figure 33. Input Logic Threshold vs. Temperature

FAN7380

SWITCHING TIME DEFINITIONS

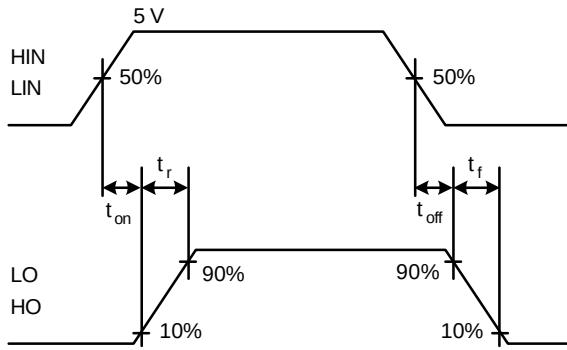


Figure 34. Switching Time Waveforms

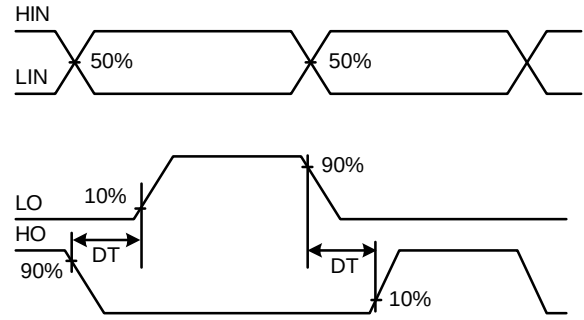


Figure 35. Internal Dead-Time Timing

ORDERING INFORMATION

Device	Package	Operating Temperature	Description	Shipping [†]
FAN7380MX (Note 5)	SOIC8 (8-SOP) (Pb-Free)	-40°C~+125°C	Lightning Application	3000 / Tape & Reel

5. This device has passed wave soldering test by JESD22A-111.

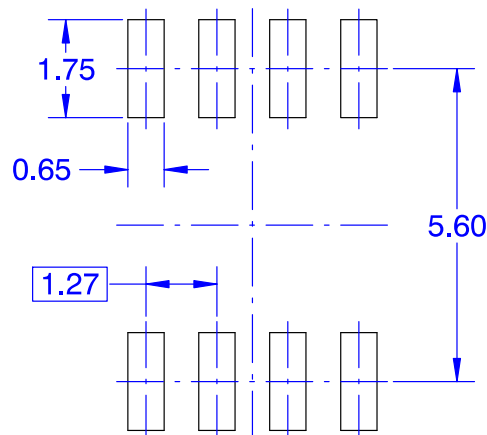
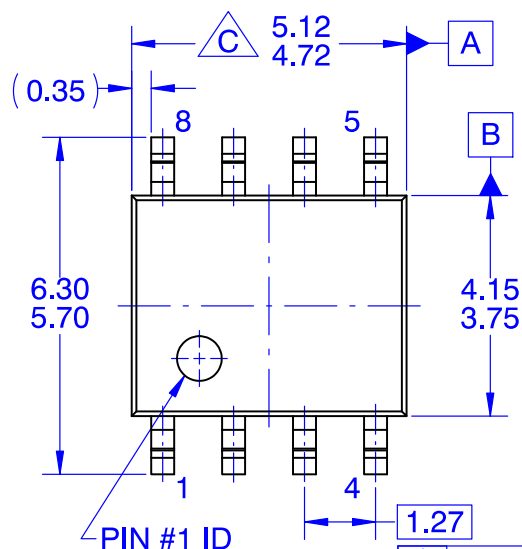
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC8

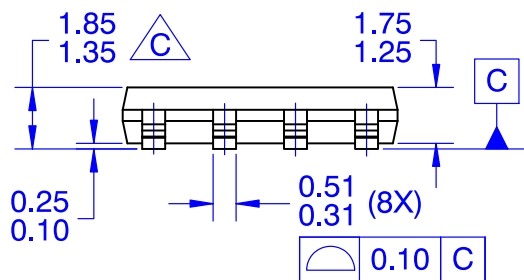
CASE 751EG

ISSUE O

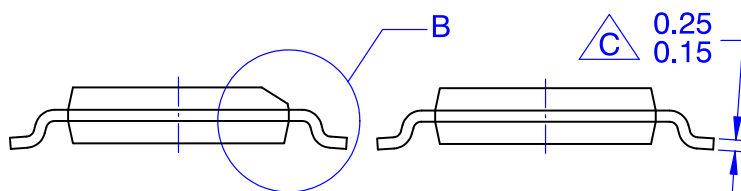
DATE 30 SEP 2016



LAND PATTERN RECOMMENDATION



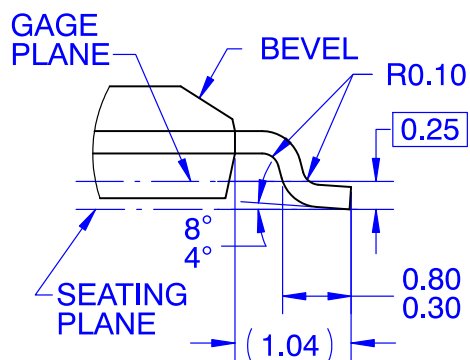
FRONT VIEW



OPTION A
BEVEL EDGE

OPTION B
NON-BEVEL EDGE

SIDE VIEW



DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE CONFORMS TO JEDEC MS-012 VARIATION A EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. OUT OF JEDEC STANDARD VALUE
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- E. LAND PATTERN AS PER IPC SOIC127P600X175-8M

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